TSC8-75 Board for ETOS

The TSC8-75 board is a proprietary piece of hardware for the PDP-8/E required to run ETOS, EduComp's Timeshared Operating System (later called Extended Timeshared Operating System when EduComp was renamed to QuoData).

The following description of the functioning of the TSC8-75 board was derived from the TSC8.SV hardware diagnostic program (available on the ETOS disk images; to convert them to the image format required for the PDP-8/E Simulator, use these download links: etosv5b-demo.rk05, etosv5b-pl5-config.rk05, etosv5b-pl5-dist.rk05), from the ETOS manuals (testing the ETOS board is described in the System Manager Guide chapter 2.11, pp. 2-41 - 2-48) and the ETOS white paper. The functioning was verified by implementing a TSC8-75 device for the PDP-8/E Simulator that now successfully runs the TSC8.SV hardware diagnostics and ETOS.

The TSC8-75 provides the following registers:

- An enable flag. When it is cleared, the PDP-8/E works as usual. When it is set, the TSC8-75 is operational.
- An interrupt flag. When the TSC8-75 and interrupts are enabled and this flag is set, an interrupt occurs.
- A 12-bit register holding the opcode of the last JMS, JMP, IOT, HLT or OSR instruction performed by the PDP-8/E running in user mode. We refer to it with the name **ERIOT register** (the original name is unknown).
- A 12-bit register holding the address of the last JMS or JMP instruction performed by the PDP-8/E running in user mode. We call it the **ERTB register** (the original name is unknown).
- A 1-bit register that is set whenever a CDF opcode (62x1) is loaded into the ERIOT register. It is cleared when any other opcode is loaded into the ERIOT register or when a ECDF or skipping ESME instruction is performed. We call it the **ECDF flag** (the original name is unknown).

Every TSC8-75 provides the following IOT instructions (at I/O address 36). The mnemonics were retrieved from the error messages of the TSC8.SV diagnostics.

Mnemonic	Opcode	Description
ETDS	6360	Disable the TSC8-75 by clearing the enable and interrupt flag.
ESKP	6361	Skip the next instruction when the interrupt flag of the TSC8-75 is set.
ECTF	6362	Clear the interrupt flag of the TSC8-75.
ECDF	6363	Move ERIOT(6-8) to AC(9-11) by performing a logical OR (when ERIOT holds a CIF, CDF or CDI, this is the field number of the instruction). When the ECDF flag is set (then ERIOT holds a CDF instruction (62x1)), additionally the next instruction is skipped. The ECDF flag is cleared.
ERTB	6364	Clear AC, then move the ERTB register to AC.
ERIOT	6366	Clear AC, then move the ERIOT register to AC.
ETEN	6367	Enable the TSC8-75 by setting the enable flag.

TSC8-75 boards starting with serial number 699 additionally provide the so called **ESME feature** (see ETOS System Manager Guide chapter 3.5, pp. 3-10 - 3-11). This feature enables the software to skip the emulation of unnecessary CDF instructions when the data field of the CDF is the current field. The TSC8.SV diagnostics is supposed to test the ESME feature (when SR9=1), but it gives no indicator for what the feature actually does. Inspecting the interrupt service routine of ETOS shows that the ESME feature is implemented by the IOT 6365 (this is the first instruction in the interrupt service routine), refered by the mnemonic ESME (the original mnemonic is unknown):

Mnemonic	Opcode	Description
ESME	6365	Serial number of TSC8-75 board before 699: NOP Serial number of TSC8-75 board 699 or higher: Skip the next instruction when the ECDF flag is set (then the ERIOT register contains a CDF opcode (62x1)) and the target data field of this CDF in ERIOT(6-8) is equal to SF(4-6), the data field that was active before the last interrupt. When a skip occurs, the ECDF flag is cleared, otherwise not.

When a TSC8-75 board is installed in a PDP-8/E, the following instructions behave not as usual when executed while the processor is running in user mode:

- HLT (7402), OSR (7404) and microprogrammed combinations with HLT and OSR: Additional to raising a user mode interrupt, the current OPR opcode is moved to the ERIOT register and the ECDF flag is cleared.
- IOT (6xxx): Additional to raising a user mode interrupt, the current IOT opcode is moved to the ERIOT register. When the IOT is a CDF instruction (62x1), the ECDF flag is set, otherwise it is cleared.
- JMP (5xxx): The current JMP opcode is moved to the ERIOT register, the ECDF flag is cleared. The address of the JMP instruction is loaded into the ERTB register and the TSC8-75 I/O flag is raised. Then the JMP is performed as usual (including the setting of IF, UF and clearing the interrupt inhibit flag).
- JMS (4xxx): The current JMS opcode is moved to the ERIOT register, the ECDF flag is cleared. The address of the JMS instruction is loaded into the ERTB register and the TSC8-75 I/O flag is raised. When the TSC8-75 is enabled, the target addess of the JMS is loaded into PC, but nothing else (loading of IF, UF, clearing the interrupt inhibit flag, storing of the return address in the first word of the subroutine) happens. When the TSC8-75 is disabled, the JMS is performed as usual.

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$Id: TSC8-75_doc.html,v 1.7 2013/02/28 17:41:34 bb Exp $